Digital to Analog Converter Design

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Content

The tutorial will concentrate on D/A converter design in MOS process technologies and cover these three broad topics.

1) A brief look at Digital to Analog conversion first principles including a description of the D/A function and the key specifications that define the performance of a D/A.

2) Common D/A architectures will be explored with these first principles in mind. The advantages and disadvantages of each will be discussed.

3) Case studies of example CMOS implementations will be included.
D/A Converter Applications

Used at the end of a digital processing chain where analog signals are required.

- **Digital Audio**
  - CD / MP3 Players, HD radio, Digital telephones
- **Digital Video**
  - DVD Players, DTV, Computer displays
- **Industrial Control Systems**
  - Motor control, valves, transducer excitation
- **Waveform Function Generators, test equipment**
- **Calibration / tuning in embedded systems, built-in self test**
D/A Transfer function

Analog output is represented as a fraction of the Reference

\[ A_o = \frac{D_i}{2^N} R_{ef} \]

Where:
- \( A_o \) = Analog output
- \( D_i \) = Digital input code
- \( N \) = Number of digital input bits (resolution)
- \( R_{ef} \) = Reference Value (full-scale)
D/A Transfer function
(graphic form)

Offset error

Gain error

Digital Input Code

Ideal relationship

1 LSB

0 001 010 011 100 101 110 111

0 1/8 2/8 3/8 4/8 5/8 6/8 7/8

Full Scale

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D/A Transfer function

Integral Nonlinearity (INL)
The maximum deviation of the analog output from the ideal straight line passing through the end points

Differential Nonlinearity (DNL)
The maximum deviation of the difference in the analog output between two adjacent codes from the ideal step size

Monotonicity
A D/A is monotonic if the output either increases or remains constant as the input code increases
Digital Input can’t precisely represent continuous analog output: Quantization Noise

The noise power due to quantization is:

\[ q^2 / 12 \]

Where:
- \( q = 1 \) LSB
- 1 LSB = Full-scale Span / \( 2^N \)

\[ \text{SNR} = N \times 6.02 \text{ dB} + 1.7 \text{ dB} \]

(quantization noise limit)

quantization noise error

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D/A First Principles

What Components do we need:

• Reference
  • May be either Voltage or Current

• Reference Divider (Voltage or Current, Time)
  • May be Resistor, Capacitor, or Transistor based

• Switches and, or combiner
MOS device as a voltage switch

NMOS I/V curves

For accurate transfer of the Voltage, \( V_{\text{source}} \) should equal \( V_{\text{drain}} \), i.e. current through switch should be zero.

For NMOS, \( V_{\text{control}} \) should be much greater than \( V_{\text{output}} \).

For a fixed gate voltage, \( R_{\text{on}} \) of switch will depend on \( V_{\text{output}} \).

![NMOS I/V curves graph]
MOS device as a voltage switch
PMOS I/V curves

For accurate transfer of the Voltage, $V_{source}$ should equal $V_{drain}$, i.e. current through switch should be zero.
For PMOS, $V_{control}$ should be much less than $V_{output}$.
For a fixed gate voltage, $R_{on}$ of switch will depend on $V_{output}$.

![Diagram showing MOS device as a voltage switch with voltage mode control and output connections. The graph shows PMOS I/V curves with voltage on the x-axis and current on the y-axis.](image-url)
MOS device as a current switch
NMOS I/V curves

For accurate transfer of the Current, \( I_{\text{source}} \) should equal \( I_{\text{drain}} \), i.e. leakage current to control node should be zero
For NMOS, \( V_{\text{control}} \) should be equal to or greater than \( V_{\text{output}} \)
When sinking current, \( V_{gs} \) will be what ever is needed to support \( I_{\text{ref}} \)
MOS device as a current switch
PMOS I/V curves

For accurate transfer of the Current, \( I_{\text{source}} \) should equal \( I_{\text{drain}} \), i.e. leakage current to control node should be zero.
For PMOS, \( V_{\text{control}} \) should be equal to or less than \( V_{\text{output}} \).
When sourcing current, \( V_{gs} \) will be what ever is needed to support \( I_{\text{ref}} \).
D/A First Principles
MOS device as a switch

Things to keep in mind when using MOS device as a switch.

1. Will the switch have current flowing through it?
2. If so, which direction source, sink, or both?
3. Where is the on/off control voltage with respect to the input and output of the switch?
D/A First Principles
Time Reference Divider

“One Bit” DAC
Pulse Width Modulation

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D/A First Principles
Voltage Reference Divider

Standard resistor divider uses $2^N$ equal resistors (and switches).

Vout must be buffered to drive a load.

R/2R ladder uses fewer unit resistors ($3N+1$), but current flows through switches, so Ron is of concern.
D/A First Principles
Current Reference Divider

All the switches are referenced to the same voltage

Voltage at I_{out} must equal V_{gnd}

Ron of switch is in series with 2R leg.
Ron should be small with respect to 2R.
Should Ron be constant, or scaled with bit position?

R/2R ladder can be used for current division as well
D/A First Principles

R/2R driven with equal currents

Alternatively, R/2R ladder can be driven at each splitting node.

Simple to make all currents and switches the same size and scale them with divider network.
Transistors As Current Source

• Weighted unit currents (equal or binary)
  – MOS matching is a function of gate area and gate voltage, $V_{gs} - V_{t}$
  – Statistical averaging across large collection of smaller devices will result in improved matching performance.

Pelgrom, JSSC Oct 1989
Matching of MOS Transistors

\[ V_{T0} = \text{zero bias threshold voltage} \]

\[ \sigma^2(V_{T0}) \propto \frac{A_{VT0}^2}{WL} + S_{VT0}^2 D^2 \]

\[ \beta = \mu C_{ox} \frac{W}{L} \]

\[ \sigma^2(\beta) \propto \frac{A_{\beta}^2}{WL} + S_{\beta}^2 D^2 \]

Where:

\[ A_{VT0}, A_{\beta}, S_{VT0}, S_{\beta} \] are process constants

\[ W, L \] gate dimensions,

\[ D \] distance between devices

Pelgrom, JSSC Oct 1989

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Current Source Array Layout

Simple Diagonal used for spatial averaging to remove errors from process gradients.

This method can be implemented with the fewest inter-connect layers.

![Diagram of current source array layout with source and drain connections.]

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Design Topics

CMOS Current steering D/A

- Basic structure
- Matching and DC linearity
- Output Impedance
- Switch Gate Driver
CMOS Current steering D/A

- Fine Line CMOS technologies are the process of choice for switched current D/As.
- Thermometer coding and unit elements used extensively to improve DNL and reduce non-linear output glitches.
- D/As with resolutions from 8 bits to 16 bits are split into two or more segments.
- PMOS current sources and switches have been more common than NMOS.
CMOS D/A Basic Structure

Three major functional blocks:
1) CMOS decode Logic / Clock / switch drivers
2) Output current source array
3) Analog bias blocks, Band-gap reference
## Comparison of Segmentation Approaches

<table>
<thead>
<tr>
<th>Paper Reference</th>
<th>Segmentation</th>
<th>Process node</th>
<th>14 bit DNL</th>
<th>14 bit INL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mercer, 1996</td>
<td>5 – 4 – 3 (5)</td>
<td>0.6u</td>
<td>+4.0 LSB</td>
<td>-3.6 LSB</td>
</tr>
<tr>
<td>Mercer, 2006</td>
<td>5 – 4 – 5</td>
<td>0.18u</td>
<td>-2.6 LSB</td>
<td>+3.0 LSB</td>
</tr>
<tr>
<td>Schafferer, 2004</td>
<td>6 - 8</td>
<td>0.18u</td>
<td>-0.7 LSB</td>
<td>-1.2 LSB</td>
</tr>
<tr>
<td>Lin, Dec. 1998</td>
<td>8 - 2</td>
<td>0.35u</td>
<td>-1.6 LSB</td>
<td>-3.6 LSB</td>
</tr>
<tr>
<td>Van der Plas, 1999</td>
<td>8 - 6</td>
<td>0.5u</td>
<td>+0.15 LSB</td>
<td>+0.3 LSB</td>
</tr>
</tbody>
</table>

(Un-calibrated)
Chip Photographs

AD9764 (1995)  
2 mm  
0.6u process

AD9707 (2005)  
1.5 mm  
0.18u process
Current Source Architecture

- 5-4-5 Segmentation
- Splitter servo matches MSB current source bias
- Monotonicity guaranteed if MSB currents match

Schofield, et al., ISSCC, 2003

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Topics

CMOS Current steering D/A

• Basic structure
• Matching and DC linearity
• Output Impedance
• Switch Gate Driver
Scaling PMOS current sources

• Larger $V_{gs} - V_t \rightarrow$ Better Matching, but larger supply headroom required
  – 0.6u, 5V supply, $V_{gs} - V_t = 600$ mV (AD9764,54)
  – 0.35u, 3.3V supply, $V_{gs} - V_t = 450$ mV (AD9744)
  – 0.18u, 1.8V supply, $V_{gs} - V_t = 260$ mV (AD9707)

• PMOS $V_t$ scaling also helps headroom,
  – 0.6u, $V_t = 935$ mV
  – 0.18u, $V_t = 675$ mV (thick oxide device)
Linearity From Raw Matching

INL (14b) vs Code

DNL (14b) vs Code

(0.18u process)

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Self Calibration

- 6b 2-4 segmented CALDAC
- Cascode bias switched to replica
- 6b SAR calibrates to 14b in two steps:
  1. Master calibrated to mid-scaled MSB source
  2. MSBs, ISB-LSB sub-DAC calibrated to master

Schofield, et al., IEEE ISSCC, Feb 2003
6 Bit Calibration DAC

- MP1: 512 LSBs
- MP2: 16 LSBs
- Return current common to all Cal DACs
- • +/- 8 LSB trim range
- • Discarded current returned to voltage equal to drain of MP1 to insure proper current split

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Self Calibrated INL/DNL

- 0.25 LSB calibration resolution should at best provide 0.25 LSB DNL
Calibration DAC Values

- Device calibrated at three temperatures.
- 25C distribution 7 codes majority in just three.
- 85C distribution tighter at 4 codes.
- Wider at -40C due in part to temperature dependence of mobility.
- Center shift due to comparator offset shift.
Topics

CMOS Current steering D/A

- Basic structure
- Matching and DC linearity
- Output Impedance
- Switch Gate Driver
Code Dependent Output Impedance

Varying numbers of $R_{sw}$ in parallel with $R_L$ results in a non-linear output voltage.

Aim is to make $R_{sw}$ much larger than $R_L$.
Code Dependent Output Impedance

\[ INL = \frac{I_{\text{unit}} R_L^2 N_u^2}{4 R_{sw}} \]

Where:
- \( I_{\text{unit}} \) is the magnitude of the unit current source
- \( R_L \) is the load impedance
- \( N_u \) is the number of unit current elements
- \( R_{sw} \) is the impedance of a unit current source

What we actually need to know is \( R_{sw} \) to design the DAC unit element. Rearranging the formula gives us the required \( R_{sw} \) for a given overall DAC resolution and \( \frac{1}{2} \) LSB INL error:

\[ R_{sw} = R_L N_u 2^{N_R - 1} \]

Where:
- \( R_L \) is the load impedance
- \( N_u \) is the number of unit current elements
- \( N_R \) is the number of bits for the overall DAC
Code Dependent Output Impedance

- $Z_{out} = (\text{code dependent } Z_{sw}) \parallel Z_L$
- # elements changing in a sinewave $\rightarrow$ diff IMD
- Pole/Zero analysis for IMD in range of interest
  - Double cascode provides best IMD

Van den Bosch, et al., *Proc. ICECS*, 1999

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Active Second Cascode

- Back gate bias of MP3,4,5,8 a function of AVDD
- Active cascode, MP3, driven to maintain Vds just in saturation for all AVDD

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Topics

CMOS Current steering D/A

- Basic structure
- Matching and DC linearity
- Output Impedance
- **Switch Gate Driver**
Driving The Current Switch

- $V_{SB}$ generator mimics switch diode to ground
  - Limits swing to be no more than needed
- Low switch crossover $\rightarrow$ constant $Z_{SWITCH}$
  - Constant $Z_{SWITCH} = \text{low } V_{CS}/\text{output glitch energy}$
    = symmetric output $\rightarrow$ low HD2

Mercer, *IEEE JSSC*, vol. 29, no. 10, October 1994

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Sensitivity to $V_{SB}$ Activity

- Would like to have local $V_{sb}$ generator for isolation
- Local $V_{SB} =$ Small Area, Low Power
  Low Power = High $Z_{OUT}$ $\rightarrow$ long settling time
- Incomplete settling at high activity = code dependent switching delay
Switch Driver Bias

- $V_{SB}$ generator, MP1 mimics switch diode with respect to ground
- MN1 (Bias2) sets current level
- Feedback through MN2 helps transient recovery

Mercer, *IEEE JSSC*, vol. 29, no. 10, October 1994
Output Current Switch Driver

- NMOS switches (MN1,4) draw pulse of current from driver bias.
- PMOS devices replace current pulse from VDD.
- Net current supplied by bias much smaller leading to lower standing current while also providing faster recovery time.
- Power more dynamic, now more a function of sample rate and data pattern.
### Performance Summary

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Max $F_{\text{sample}}$</td>
<td>200</td>
<td>MS/s</td>
</tr>
<tr>
<td>Resolution</td>
<td>14</td>
<td>bits</td>
</tr>
<tr>
<td>DNL</td>
<td>&lt;1</td>
<td>LSB</td>
</tr>
<tr>
<td>INL</td>
<td>&lt;1</td>
<td>LSB</td>
</tr>
<tr>
<td>SFDR (at 10MHz)</td>
<td>78</td>
<td>dBc</td>
</tr>
<tr>
<td>IMD (to 70MHz)</td>
<td>&lt;-70</td>
<td>dBc</td>
</tr>
<tr>
<td>NSD</td>
<td>&lt;-150</td>
<td>dBm/Hz</td>
</tr>
<tr>
<td>Glitch impulse</td>
<td>&lt; 6</td>
<td>pVSec</td>
</tr>
<tr>
<td>Power (1.8V)</td>
<td>12.5</td>
<td>mW</td>
</tr>
<tr>
<td>Area (including bond pads)</td>
<td>1.5X1.5</td>
<td>mm</td>
</tr>
</tbody>
</table>
D/A First Principles

What Components do we need:

- Reference
  - May be either Voltage or Current
- Reference Divider (Voltage or Current)
  - May be Resistor, Capacitor, or Transistor based
- Switches and, or combiner
- A bunch of support circuitry to make it all work
References

• [8] D. Mercer; “A Low Power Current Steering Digital to Analog Converter in 0.18 micron CMOS”, ISLPED 2005 Digest of Technical Papers, pp. 72-77

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References

- [31] AD9754 data sheet
- [32] AD9744 data sheet
Extra slides
Switched Current DACs
Power vs. Time

[1] AD9713 100 MSPS 12 bit DAC

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Switched Current DACs
SFDR vs. Time

- 1 MHz SFDR
- Max Freq reported or 50 MHz SFDR

[1] AD9713
CMOS Process Scaling

- Process scaling impacts digital logic power consumption
  - 0.6u 12 bits, thermometer code, 0.3 mW / MSPS @5V[2]
  - 0.18u 14 bits, thermometer code, 0.18 mW / MSPS @3.3V[6]
  - 0.18u 14 bits, thermometer code, 0.04 mW / MSPS @1.8V[6]
  - 0.18u 10 bits, binary code, 0.016mW / MSPS @1.5V[5]
- 86% reduction comparing [2] and [6]
Analog Power Scaling

• Supply voltage has decreased over time
  – 5V > 3.3V > 2.5V > 1.8V (factor of 0.36)

• Full scale output current reduced from 20 to 2mA

• Power consumed in analog bias circuits impact SFDR performance
  – 0.6u DAC, no cascode, 5 mA bias current
    SFDR 61 dBC at 10 MHz (AD9764)
  – 0.6u DAC, with cascode, 12 mA bias current
    SFDR 73 dBC at 10 MHz (AD9754)
  – 0.18u DAC, two level cascode, 2.5 mA bias current
    SFDR 77 dBC at 10 MHz (AD9707)